What is Claimed is:

1. A programmable logic resource comprising digital signal processing circuitry, the digital signal processing circuitry comprising:

at least one multiplier configured with the capability to perform rounding and saturation on a respective output of the at least one multiplier.

2. The programmable logic resource of claim 1 wherein the digital signal processing circuitry is a multiply-accumulate block.

3. The programmable logic resource of claim 1 further comprising at least one add-subtract-accumulate circuit configured with the capability to perform rounding and saturation on a respective output of the at least one add-subtract-accumulate circuit.

4. The programmable logic resource of claim 1 wherein the at least one multiplier is configured with the capability to perform rounding and saturation based on a 1.15 format.

5. A programmable logic resource comprising:

at least one multiplier implemented using digital signal processing circuitry, the at least one multiplier comprising:

multiplication circuitry that multiplies inputs to the multiplier,

shifting circuitry coupled to the multiplication circuitry that shifts bits of an output of the multiplication circuitry,

adder circuitry coupled to the

shifting circuitry that adds an output of the shifting circuitry with a predefined value, and

zeroing circuitry coupled to the adder circuitry that zeros a predetermined number of least significant bits of an output of the adder circuitry.

6. The programmable logic resource of claim 5 wherein the digital processing circuitry is a multiply-accumulate block.

7. The programmable logic resource of claim 5 further comprising saturation circuitry coupled to the inputs to the multiplier, the adder circuitry and the zeroing circuitry, wherein the saturation circuitry is configured to determine whether the inputs to the multiplier would produce an overflow.

8. The programmable logic resource of claim 7 wherein if the inputs to the multiplier would produce an overflow, the saturation circuitry outputs to the input of the zeroing circuitry a saturated value.

9. The programmable logic resource of claim 5 wherein the inputs to the multiplier are in a 1.15 format.

10. The programmable logic resource of claim 9 wherein the output of the shifting circuitry is in a 1.31 format.

11. The programmable logic resource of claim 9 wherein the predetermined value is in a 1.31 format.

12. The programmable logic resource of claim 9 wherein the predetermined value is 0x00008000.

13. The programmable logic resource of claim 5 wherein the predetermined number of least significant bits is 16.

14. A programmable logic resource comprising digital signal processing circuitry, the digital signal processing circuitry comprising:

at least one add-subtract-accumulate circuit configured with the capability to perform rounding and saturation on a respective output of the at least one multiplier.

15. The programmable logic resource of claim 14 wherein the digital signal processing circuitry is a multiply-accumulate block.

16. The programmable logic resource of claim 14 further comprising at least one multiplier configured with the capability to perform rounding and saturation on a respective output of the at least one multiplier.

17. The programmable logic resource of claim 14 wherein the at least one multiplier is configured with the capability to perform rounding and saturation based on a 1.15 format.

18. A programmable logic resource comprising:

at least one add-subtract-accumulate circuit implemented using digital signal processing circuitry, the at least one add-subtract-accumulate

circuit comprising:

addition/subtraction circuitry that adds/subtracts inputs to the add-subtract-accumulate circuit,

adder circuitry coupled to the addition/subtraction circuitry that adds an output of the addition/subtraction circuitry with a predefined value, and

zeroing circuitry coupled to the adder circuitry that zeros a predetermined number of least significant bits of an output of the adder circuitry.

19. The programmable logic resource of claim 18 wherein the digital processing circuitry is a multiply-accumulate block.

20. The programmable logic resource of claim 18 further comprising saturation circuitry coupled to the output of the adder circuitry and the zeroing circuitry, wherein the saturation circuitry is configured to determine whether the inputs to the multiplier would produce an overflow or underflow.

21. The programmable logic resource of claim 20 wherein if the inputs to the multiplier would produce an overflow or underflow, the saturation circuitry outputs to the input of the zeroing circuitry a saturated value.

22. The programmable logic resource of claim 18 wherein the inputs to the multiplier are in a 1.31 format and an 18.31 format.

23. The programmable logic resource of claim 22 wherein the predetermined value is in a 1.31 format.

24. The programmable logic resource of claim 22 wherein the predetermined value is 0x00008000.

25. The programmable logic resource of claim 18 wherein the predetermined number of least significant bits is 16.

26. A printed circuit board on which is mounted a programmable logic resource as defined in claim 5.

27. The printed circuit board defined in claim 26 further comprising:

a memory mounted on the printed circuit board and coupled to the memory circuitry.

28. The printed circuit board defined in claim 27 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

29. A printed circuit board on which is mounted a programmable logic resource as defined in claim 18.

30. The printed circuit board defined in claim 29 further comprising:

a memory mounted on the printed circuit board and coupled to the memory circuitry.

31. The printed circuit board defined in claim 30 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

5